

FORM PTO-1449 (modified)
To: U.S. Department of Commerce
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MAY 17 2002

INFORMATION DISCLOSURE STATEMENT
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Date: May 10, 2002

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U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
AR	5,361,373	11/01/94	Gilson	395	800	
BR	5,696,956	12/09/97	Razdan et al.	395	568	
CR	5,819,064	10/06/98	Razdan et al.	395	500	
DR	6,035,123	03/07/00	Razdan et al.	395	709	
ER						
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FOREIGN PATENT DOCUMENTS

	Document Number	Date MM/YYYY	Country	Inventor Name	English Abstract	Translation Readily Available
					Enclosed	No
OR						
PR						
QR						
RR						
SR						
TR						
UR						
VR						

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

TD	WR	Compton et al., "Configurable Computing: A Survey of Systems and Software," Technical Report, Northwestern University, Dept. of ECE, 1999
TD	XR	Hauck et al., "The Chimaera Reconfigurable Functional Unit," Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines, 1997
TD	YR	Razdan et al., "A High-Performance Microarchitecture with Hardware-Programmable Function Units," Proceedings of MICRO-27, November 1997
TD	ZR	Wang et al., "Hardware/Software Instruction Set Configurability for System-on-Chip Processors," Proceedings of Design Automation Conference, 2001

Examiner *Muensel*

Date Considered: **6-10-03**

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 (modified)
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INFORMATION DISCLOSURE STATEMENT
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Date: October 8, 2002

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U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
TP	AR	5,896,521	04/20/99	Shackleford et al.	395	500	
TP	BR	5,918,035	06/29/99	van Praet et al..	395	500	
CR							
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FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name	English Abstract		Translation Readily Available	
						Enclosed	No	Enclose	No
TP	MR	EP 0 743 599	11/20/96	Europe	van Praet et al.	YES			
NR									
OR									
PR									
QR									
RR									
SR									
TR									

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

TP	UR	Fauth et al., "Describing Instruction Set Processors Using nML," ED&TC 1995, Proceedings, Paris, France 6-9 March 1995, Los Alamitos, CA, USA, IEEE Comput. Soc. US, 6 March 1995, pp. 503-507
TP	VR	Hartoog et al., "Generation of Software Tools from Processor Descriptions for Hardware/Software Codesign," Proceedings of the Design Automation Conference, Anaheim, CA, USA, June 9-13, 1997, pp. 303-306
TP	WR	Fauth et al., "Generation of Hardware Machine Models from Instruction Set Descriptions," VLSI Signal Processing, VI, 1993, Workshop on Veldhoven, Netherlands, 20-22 Oct. 1993, New York, NY, USA, IEEE, 20 October 1993, pp. 242-250
	XR	

Examiner *Murando* Date Considered: *6/10/03*

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